REMARKS

Claims 19-36 are pending.

Claims 19-36 stand rejected.

Claim 37 has been added.

No new matter has been added.

Claims 19-37 are hereby submitted for reconsideration.

In paragraph 3 of the Office Action, the Examiner has rejected claims 19-36 under 35 U.S.C. § 103 as being unpatentable over Reader et al. (U.S. Patent No. 6,192,073) in view of Kusters (U.S. Patent No. 5,819,112). The Examiner contends that Reader teaches all of the elements of the present invention except for a multiplexer coupled to the interface for providing access between a selected number of I/O device driver units to external I/O devices via output pins. However, the Examiner contends that Kusters teaches such an element and that it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the multimedia processor of Reader with the multiplexer of Kusters to arrive at the present invention as claimed.

In paragraph 6 of the Office Action, the Examiner has alternatively rejected claims 19-36 under 35 U.S.C. § 103 as being unpatentable over Reader et al. (U.S. Patent No. 6,192,073) in view of Kim (U.S. Patent No. 5,926,187).

In paragraph 12 of the Office Action, the Examiner has provisionally rejected claims 19-36 under the judicially created doctrine of obviousness type double patenting as being

unpatentable over claims 1-18 of co-pending U.S. Patent Application No. 09/172,286.

Applicants respectfully disagree with the Examiner's contentions and submit the following remarks in response.

The present invention is directed to an integrated multimedia system having a multimedia processor disposed in an integrated circuit, wherein the multimedia system comprises a first host processor system coupled to the multimedia processor. A second local processor is disposed within the multimedia processor for controlling the operation of the multimedia processor. A data transfer switch is disposed within the multimedia processor and coupled to the second processor for transferring data to various modules of the multimedia processor. A data streamer is coupled to the data transfer switch, and configured to schedule simultaneous data transfers among a plurality of modules disposed within the multimedia processor in accordance with corresponding channel allocations.

An interface unit is coupled to the data streamer having a plurality of input/output (I/O) device driver units. A multiplexer is coupled to the interface unit for providing access between a selected number of I/O device driver units to external I/O devices via output pins and a plurality of external I/O devices are coupled to the multimedia processor.

In this configuration, the present invention is directed to reducing bandwidth delays by employing a data transfer arrangement that overcomes the disadvantages of the prior art utilizing a data streamer and interface unit which allow the data transfer switch to transfer information to a number of external I/O devices simultaneously. In addition, in order to further enhance data transfer rates to support graphics processing, the CPUs in the multimedia processor are directly coupled to the cache memory rather than first passing through a data transfer switch.

The cited prior art, namely Reader, teaches a method and apparatus for processing video data using three processors capable to operate concurrently, a scaler processor, a vector processor and a bit stream processor. As illustrated in Fig. 17, the three CPUs (scaler, vector and bitstream) utilized in the Reader video processor maintain cache RAM and cache ROM connections across a data path pipeline (area enclosed by the dotted line in Fig. 17). In this configuration, the CPU's must transmit data across the data transfer switch in order to access the cache.

Additionally, the bit stream processor 245 in Fig. 2 of the Reader reference, as described in column 5 lines 4-21, is connected between the vector processor and the scaler processor and configured to transfer calculated results to the scaler processor. Column 5, lines 4-21 of Reader states:

> "Examples of encoding and decoding operations are given in Appendix A, Sections 10.6.1 and 10.6.2...In some embodiments, device interface circuit 252 includes a video A/D converter, and the uncompressed data arrive from the converter. Vector processor 220 performs quantization, DCT, and motion compensation. Bitstream processor 245 receives the output of VP 220 and produces GOBs (Groups of Blocks) or slices. In particular, BP 245 performs Huffman and RLC encoding and zig-zag bitstream processing. Scalar processor 210 receives the output of BP 245 and performs picture layer coding, GOP (group of pictures) coding, and sequence layer coding. Scalar processor 210 then multiplexes audio and video data and transfers the coded data to a storage device (via bus 105 or 122) or a network. Transfer to a network involves transfer to device interface circuit 252 which is connected to a network in some embodiments."

Thus, as described, the bit stream processor of Reader is an encoding and decoding device which acts to processes data.

The cited prior art, namely Kusters, teaches an apparatus for controlling and I/O port by queuing requests and in response to a predefined condition, enabling the I/O port to receive the interrupt requests. The Kusters reference provides a system and method for controlling parallel

port peer to peer communication in personal computers.

The cited prior art, namely Kim, teaches video interface and overlay system and process. The Kim reference is directed to overcoming drawbacks in the prior art associated wit inserting multiple video images into multiple video windows in the graphics images by providing a system for enhanced matching of video windows with video signals or video pixel maps.

Contrary to the Examiner's contentions, there is no teaching or suggestion in any of the cited prior art which discloses the present invention as claimed. For example, there is no teaching or suggestion in the cited prior art, either alone or in combination which teaches a data streamer coupled to the data transfer switch, and configured to schedule simultaneous data transfers among a plurality of modules disposed within the multimedia processor in accordance with corresponding channel allocations. Unlike the data streamer of the present invention, the bitstream processor of Reader cited by the Examiner, is not configured to schedule simultaneous data transfers among a plurality of modules within the multimedia processor but rather to perform encoding and decoding processing on video data. Additionally, the WDM Streaming media software also cited by the Examiner as teaching the data streamer of the present invention in no way describes or maintains the ability to schedule simultaneous data transfers among a plurality of modules within the multimedia processor, in accordance with corresponding channel allocation.

Likewise, there is no teaching or suggestion in any of the cited prior art, either alone or in combination, which teaches or suggests a cache memory directly coupled to the first host processor system, the second local processor and the data transfer switch. As discussed above the cache memory of Reader is connected to the CPU across a data path pipeline switch, unlike

the present invention where the cache system is connected to the data transfer switch and also is directly coupled to the first host processor system and the second local processor.

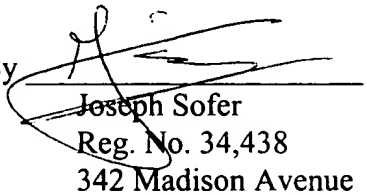
Therefore, Applicants respectfully submit that none of the cited prior art references, either alone or in combination, teach or suggest the present invention as claimed. As such, Applicants respectfully request that the rejection under 35 U.S.C. § 103 of independent claims 19 and 28 and claims 20-27 and 29-37 which depend therefrom be withdrawn.

Applicants note that Application No. 09/172,286 has since issued as U.S. Patent No. 6,347,344 on February 12, 2000. Applicants will respond to the issue of double patenting with a Terminal Disclaimer after all other rejections have been removed.

In view of the aforementioned amendment and remarks, it is respectfully submitted that all claims currently pending in the above identified application are now in condition for allowance, the earliest possible notice of which is earnestly solicited. If in the Examiner's opinion the prosecution of the present application would be advanced by a telephone interview, he is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,

SOFER & HAROUN, L.L.P.

By 

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